UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/772,590 | 02/04/2004 | Roberto Pelliconi | 361181-1011 | 2338 |

32914 7590 11/13/2009

GARDERE WYNNE SEWELL LLP
INTELLECTUAL PROPERTY SECTION
3000 THANKSGIVING TOWER
1601 ELM ST
DALLAS, TX 75201-4761

| EXAMINER | |
|---|---|
| PUENTE, EVA YI ZHENG | |
| ART UNIT | PAPER NUMBER |
| 2611 | |
| MAIL DATE | DELIVERY MODE |
| 11/13/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/772,590 | PELLICONI ET AL. | |
| | Examiner | Art Unit | |
| | EVA Y. PUENTE | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-10,14,16,17,19,22,23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10, 14, 16-17, 19, 22-23, and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see Amendment, filed 7/2/09, with respect to the rejection(s) of claim(s) 2-10, 14, 16-17, 19, 22-23, and 25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

### *Claim Objections*

2. Claim 22 is objected to because of the following informalities: on line 16, please change "communications" after "second" to -- communication --. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable by Upp (US 5,901,146) in view of Lincoln (US 2005/0069041).

a) Regarding claim 4, Upp discloses a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block

(bus master 100 in Fig. 5) and a receiver block (user 112) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data on bus 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (CONJ bus 128);

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data signal comprises a new datum (new data is inherent since data line is bi-directional and transmitted continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L25-49; no "FRAME" communication when request is not granted).

Upp discloses data communication between a transmitter and receiver device. Upp did not explicitly disclose the transmitter and the receiver device has a different sampling period.

However, Lincoln discloses communicating data between a transmitter and a receiver device (74 and 76 in Fig. 5). The receiver device comprising delay registers and samples the transmission signal at a different sampling time ([0049]). Thus, the receiving device allows the receiver to correct for any phase delays associated with the transmission lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the data communication system of Upp with the different sampling period of Lincoln to indicates the transmitter and

receiver device has different sampling period. One of ordinary skill in the art would be motivated to do so to accommodate large number of parallel data lines with high speed communication between two physical devices.

b) Regarding claim 5, Upp discloses a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block (bus master 100 in Fig. 5) and a receiver block (user 112) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data on bus 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal (CONJ bus 128);

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data signal comprises a new datum (new data is inherent since data line is bi-directional and transmitted continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L25-49; no "FRAME" communication when request is not granted).

Upp discloses data communication between a transmitter and receiver device. Upp did not explicitly disclose the transmitter and the receiver device has a different sampling period.

However, Lincoln discloses communicating data between a transmitter and a receiver device (74 and 76 in Fig. 5). The receiver device comprising delay registers and samples the transmission signal at a different sampling time ([0049]). The delays in the receiver device indicate a shorter sampling period than the transmission period of the transmitter block. Thus, the receiving device allows the receiver to correct for any phase delays associated with the transmission lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the data communication system of Upp with the different sampling period of Lincoln to indicates the transmitter and receiver device has different sampling period. One of ordinary skill in the art would be motivated to do so to accommodate large number of parallel data lines with high speed communication between two physical devices.

5. Claims 2, 3, 14, 16, 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable by Upp (US 5,901,146) in view of Cagenius (US 7,047,028).

a) Regarding to claims 2 and 25, Upp discloses a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block (100 in Fig. 5) and a receiver block (112 in Fig. 5) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data bus line 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver bloc occurs in order to interrupt the transmission of said data signal (CONJ bus line 128; Col 6, L44-49); and

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data signal on the first line comprises a new datum (it is inherent since Data bus line is bi-directional and transmit continuously),

wherein the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L44-49).

Upp disclose all the subject matters above except for the specific teaching of a delay in the synchro signal with respect to the data signal.

However, Cagenius discloses data and frame sync signals in a communication system, wherein the frame sync is delayed by a predetermined amount along with the data to preserve the timing relationship between the frame sync and the data (Fig. 4A; Col 9, L6-20). A timing controller (52) measures the up-to-date delay and ensures delay compensation accuracy (Col 10, L37-41). Therefore, it is obvious to one of ordinary skill in the art at the time of invention was made to combine the time delay of frame synch signal of Cagenius with the data communication system of Upp. Thus indicate synchro signal is delayed for communication over the third line with respect to the data signal which is communication over the first line. By doing so, ensure channel condition measurement accuracy in a data interchanging communication system.

b) Regarding to claim 3, Upp did not explicitly teach the syncrho signal is delayed

half transmission period. However, Cagenius discloses timing delay in the frame sync signal. Therefore, it is obvious to one of ordinary skill in the art at the time of invention was made to combine the time delay of frame synch signal of Cagenius with the data communication system of Upp, and set time delay of frame synch signal at a half transmission period with respect to the data signal. By doing so, accurately control data interchange communication system.

c) Regarding to claim 14, Upp discloses a communication protocol method, comprising: transmitting from a transmitting entity (100 in Fig. 5) to a receiving entity (112 in Fig. 5) along with a data signal (Data bus line 118) and a synchronization signal (FRAME bus line) indicating to the receiving entity that the data signal comprises new datum (it is inherent since Data bus line is bi-directional and transmit continuously); and

inhibiting transmission of the synchronization signal by the transmitting entity in response to an indication received from the receiving entity of the existence of a congestion condition at the receiving entity (CONJ bus line 128; Col 6, L44-49; no "FRAME" communication when request is not granted),

wherein the data signal is communicated on a first communication line and the synchronization signal is communicated on a second communication line (Fig. 5).

Upp disclose all the subject matters above except for the specific teaching of a delay in the synchro signal with respect to the data signal.

However, Cagenius discloses data and frame sync signals in a communication system, wherein a timing delay in the frame sync signal is measured. The amount of delay depends on channel conditions and is independent from data signal (Fig. 5; Col

10, L28-41). Therefore, it is obvious to one of ordinary skill in the art at the time of invention was made to combine the time delay of frame synch signal of Cagenius with the data communication system of Upp. Thus indicate synchro signal is delayed for communication over the third line with respect to the data signal which is communication over the first line. By doing so, ensure channel condition measurement accuracy in a data interchange communication system.

d) Regarding to claim 16, Upp discloses the protocol method as in claim 14, wherein the indication of the existence of a congestion condition at the receiving entity is received over a third communication line (Fig. 5).

e) Regarding to claim 17, Upp discloses the protocol method as in claim 14 further including inhibiting transmission of the data signal in response to the indication received from the receiving entity of the existence of a congestion condition at the receiving entity (CONJ bus line 128; Col 6, L44-49).

6. Claims 6, 9, 10, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable by Upp (US 5,901,146) in view of Applicant Admitted Prior Art (AAPA).

a) Regarding to claim 6, Upp disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block (100 in Fig. 5) and a receiver block (112 in Fig. 5) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data bus line 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (CONJ bus line 128; Col 6, L44-49); and

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data signal comprises a new datum (it is inherent since Data bus line is bi-directional and transmit continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L L44-49).

Upp disclose all the subject matters above except for the specific teaching that (1) the first, second and third communication lines are each comprises a repeater device; and (2) an elementary delay must be shorter than half of the transmission period.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art at the time of invention was made to implement the repeaters of AAPA in the data transfer system of Upp. Thus indicates that the first, second, and third communication lines are split into

stages with repeaters. The first and third communication lines are being controlled by the second communication line through the repeaters. By doing so, improve and prevent data exchange error in a communication system.

In addition, AAPA discloses each stages has a time delay ([0019]; An in Fig. 1). AAPA did not specify the delay time must be shorter than half the transmission period. However, such limitation is merely matter of design choice. The delay elements implemented in the communication lines of both instant application and AAPA are used to facilitate data interchange in a communication system. The amount of delay time will not alter the system as a whole, which is to accurately transmit and received data. Therefore, it is obvious to one of ordinary skill in the art at the time of invention was made to set the delay time shorter than the half of transmission period in the data communication system of Upp. By doing so, facilitate data interchange in a communication system.

b) Regarding to claim 9, Upp disclose an integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block (100 in Fig. 5) and a receiver block (112 in Fig. 5) connected through a communication network, said communication network comprising a first line for a data signal (Data bus line 118), a second line for a congestion signal (CONJ bus line 128; Col 6, L44-49), and a third line for a synchro signal (FRAME bus line).

Upp disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). The tristate type of repeater devices (Bn) on data communication line (5a in Fig. 1) and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art at the time of invention was made to implement the repeaters of AAPA in the data transfer system of Upp. Thus indicates that the first, second, and third communication lines are split into stages with repeaters. The first and third communication lines are being controlled by the second communication line through the repeaters. By doing so, improve and prevent data exchange error in a communication system.

c) Regarding to claim 10, Upp disclose wherein said signal line comprises a couple of further lines for unidirectional signals indicating the transmission direction between said transmitter block and said receiver block (100 and 112 in Fig. 5), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block (ACK bus line 126; Col 6, L37-44).

d) Regarding to claim 19, Upp disclose a communication system, comprising:

a first communication block (100 in Fig. 5);

a second communication block (112 in Fig. 5);

a communication network interconnecting the first and second communication blocks (bus lines in Fig. 5); the communication network comprising:

a first communication line for carrying a data signal (Data bus line 118);

a second communication line for carrying a congestion signal (CONJ bus line 128; Col 6, L44-49); and

a third communication line for carrying a synchronization signal (FRAME bus line); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Col 9, L29-51).

Upp disclose all the subject matters above except for the specific teaching that the first, second and third communication line is each split into corresponding stages and comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art at the time of invention was made to implement the repeaters of AAPA in the data transfer system of Upp. Thus indicates that the first, second, and third communication lines are split into stages with repeaters. The first and third communication lines are being controlled by the second communication line through the repeaters. By doing so, improve and prevent data exchange error in a communication system.

7. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Upp (US 5,901,146) in view of Hann (US 6,965,558).

a) Regarding to claim 22, Upp disclose a communication system, comprising:

a first communication block (bus master 100 in Fig. 5);

a second communication block (user 112);

a communication network interconnecting the first and second communication blocks (bus lines as shown in Fig. 5); the communication network comprising:

a first communication line for carrying a data signal (Data on bus 118);

a second communication line for carrying a congestion signal (CONJ bus 128; Col 6, L44-59); and

a third communication line for carrying a synchronization signal (FRAME bus line); wherein the synchronization signal is active whenever the data signal on the first communication is new datum ("FRAME" and "DATA" are active when there is no congestion) and inactive whenever the congestion signal on the second communication line is active (Col 9, L29-51; no "FRAME" and "DATA" communication when there is congestion);

wherein the first and second communication lines are bi-directional (Fig. 5), further including:

a transmit signal line (CLOCK bus line)); and

a receive signal line (ACK bus line);

wherein the transmit and receiver signal lines interconnected the first and second communication blocks, and control signals thereon specify, for the bi-directional first

communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal (Col 6, L36-44; ACK and CONJ bus lines grant data communication between the master and users).

Upp did not explicitly teach the third communication line is bi-directional and including a transmit signal line and receive signal line. However, Upp discloses that the master bus and user bus are interchangeable. The user bus could be the master bus (Col 1, L28). In addition, Hann discloses data communication between a master and a slave network (Fig. 2), wherein comprises data (52), clock (36), and synch (40) bus lines, which are bi-directional (Col 3, L58-60). The master and slave network can communication in reverse directions (Col 4, L6-8). The first and second communication blocks set a logic state of the transmit signal line and received signal line for the data signal (38, 34, 44, 42, and 46). Therefore, it is obvious to one of ordinary skill in the art at the time of invention was made to combine the network communication system of Hann with the data communication system of Upp. Thus indicates the first (DATA), second (CONJ), and third communication lines (sync) are bi-directional, including a transmit signal line in one communication direction and a receive signal line in a reversed communication direction between the user bus and master bus. By doing so, facilitate data interchanging in a communication system.

b) Regarding to claim 23, Upp discloses a request signal line that interconnects the first and second communication, and a control signal thereon used to negotiate which of

the first and second communication blocks is to be transmitter/receiver (ACK bus line 126; Col 6, L36-44).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Puente whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 6, 2009

/Eva Y Puente/
Examiner, Art Unit 2611